VISCOUS PROTECTIVE OVERLAYERS FOR PLANARIZATION OF INTEGRATED CIRCUITS

ABSTRACT OF DISCLOSURE

The present invention relates to the planarization of surfaces as typically encountered in the fabrication of integrated circuits, particularly copper conductors and Ta/TaN barrier layers encountered in damascene and dual damascene interconnects. The present invention describes planarization methods for Cu/Ta/TaN interconnects, typically making use of a viscous overlayer tending to dwell in regions of lower surface topography, protecting said lower regions from etching by a combination of chemical and mechanical effects. In some embodiments, the viscous overlayer contains species that hinder removal of copper from regions of the surface in contact with the viscous layer. Such species may be a substantially saturated solution of copper ions among other additives, thereby hindering the dissolution of interconnect copper into the protective overlayer. In some embodiments of the present invention, the viscous overlayer may be added prior to the introduction of etchant to the wafer surface, or both etchant and viscous overlayer may be introduced substantially simultaneously, typically as the wafer is spun during planarization.